

FIG. 1A  
(PRIOR ART)

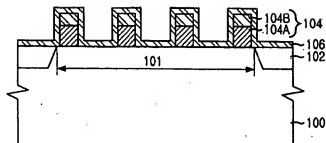


FIG. 1B  
(PRIOR ART)

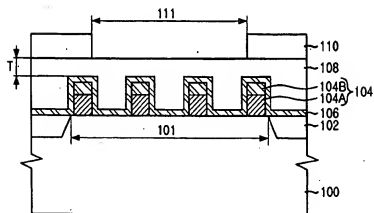


FIG. 1C  
(PRIOR ART)

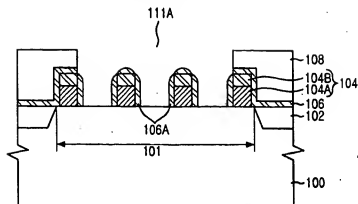


FIG. 1D  
(PRIOR ART)

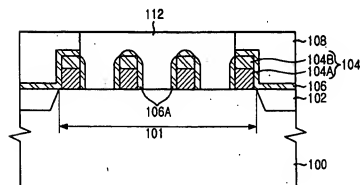


FIG. 1E  
(PRIOR ART)

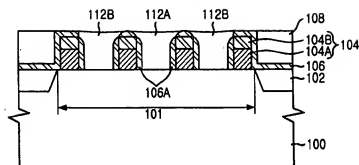


FIG. 2  
(PRIOR ART)

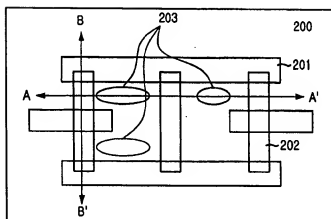


FIG. 3A  
(PRIOR ART)

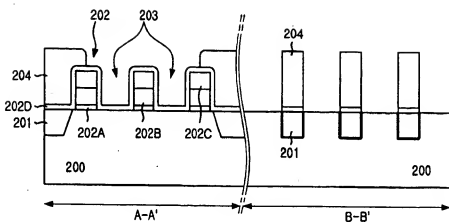
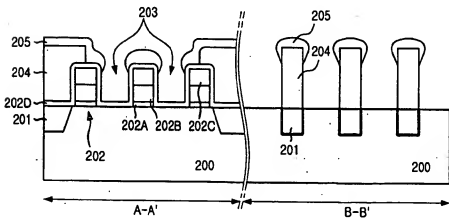


FIG. 3B  
(PRIOR ART)



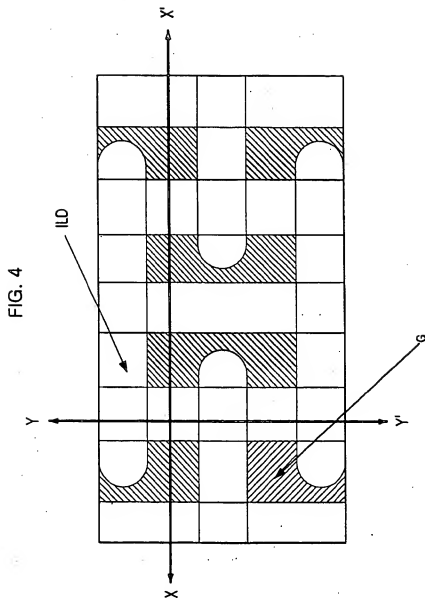


FIG. 5A

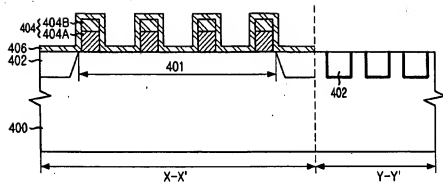


FIG. 5B

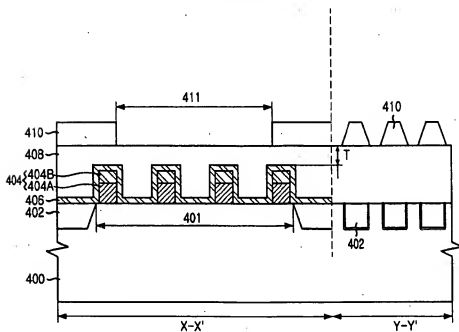


FIG. 5C

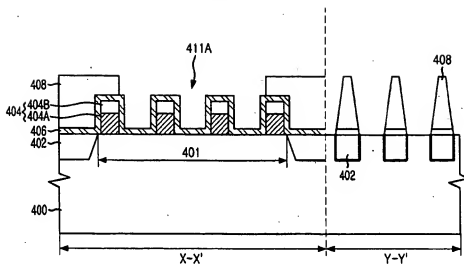


FIG. 5D

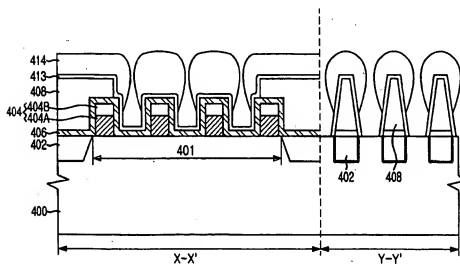




FIG. 5E

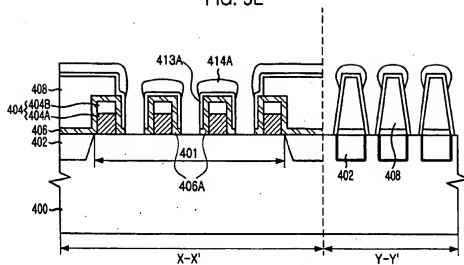


FIG. 5F

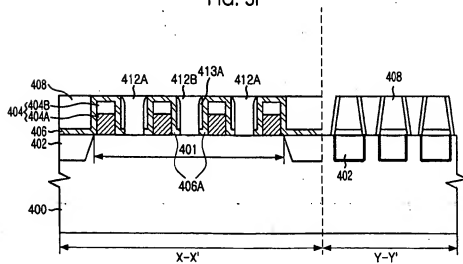


FIG. 6A

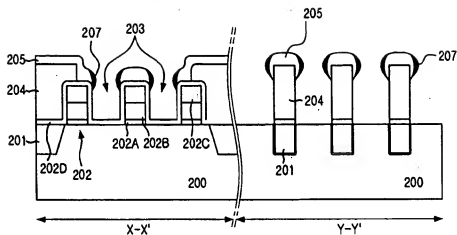


FIG. 6B

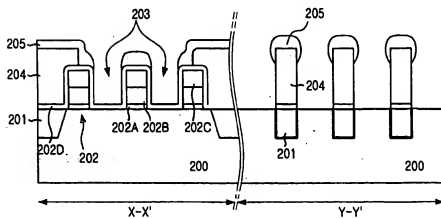


FIG. 1 is a cross-sectional view of a semiconductor device 200. The device includes a substrate 201 and a gate stack 202. The gate stack 202 is divided into regions 202A, 202B, and 202C. A gate electrode 204 is formed on top of the gate stack 202. A gate electrode 208 is also shown. The device is divided into two regions, X-X' and Y-Y'.